IEEE Transactions on Emerging Topics in Computing Special Section on Emerging Trends and Computing Paradigms for Testing, Reliability and Security in Future VLSI Systems

Guest editors:
Stefano Di Carlo (Politecnico di Torino, Italy)
Peilin Song (IBM Research, New York, NY, USA)
Alessandro Savino (Politecnico di Torino, Italy)

Corresponding TETC editor: Weiqiang Liu (NUAA, Nanjing, China)

Schedule:

- deadline for submissions: July 1, 2019
- first decision (accept/reject/revise expected): September 2, 2019
- submission of revised papers: October 1, 2019
- notification of final decision (expected): December 13, 2019

With the rapid advancement of computing technologies in all domains (i.e., handheld devices, autonomous vehicles, medical devices, and massive supercomputers), testability, reliability and security of electronic systems are crucial issues to guarantee safeness of human life. Emerging technologies coupled with new computing paradigms (e.g., approximate computing, neuromorphic computing, in-memory computing) are together exacerbating these problems posing significant challenges to researchers and designers. To address this increased complexity in the hardware testing/reliability/security domain, it is imperative to employ design and analysis methods working at all levels of abstraction, starting from the system level down to the gate level. The IEEE Transactions on Emerging Topics in Computing (TETC) seeks original manuscripts for a Special Section on Emerging Trends and Computing Paradigms for Testing, Reliability and Security in future VLSI systems. All aspects of design, manufacturing, test, monitoring and securing of systems affected by defects and malicious attacks are of interest. The relevant topics for this special section include, but are not limited to:

- Yield Analysis and Modeling: Defect/Fault analysis and models; statistical yield modeling; critical area and metrics.
- Error Detection, Correction, and Recovery: Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques, architectural-specific techniques, system-level strategies.
- Cross-layer Dependability Analysis and Validation: fault injection techniques; dependability characterization; aging modeling and analysis with emphasis on cross-layer solutions.
- Defect and Fault Tolerance: Reliable circuit/system synthesis; radiation hardened and/or tolerant processes & design; design space exploration for dependable systems, transient/soft faults and errors; aging management and recovery strategies.
- Safe design for critical applications: methodologies and case study applications to automotive, railway, avionics, industrial control, biomedicine, space and smart power networks.
- Design for Security: fault attacks, fault tolerance-based counter-measures, Scan-based attacks and counter-measures, hardware trojans, security vs reliability trade-offs, interaction between VLSI test, trust, and reliability.
- Reliable and secure systems design with emerging computing paradigms: Reliable and secure design techniques for emerging computing paradigms (e.g., approximate computing, neuromorphic computing, in-memory computing).

Submitted papers must include a new significant research-based technical contribution. The submitted papers must include a clear evaluation of the proposed solutions (based on simulation and/or implementations results) and comparisons to state-of-the-art solutions. Purely teoretical, technological or lacking methodological-and-generality papers are not suitable. For additional information please send an email to tetc.sivlsitest@gmail.com. Papers under review elsewhere are not acceptable for submission. Extended versions of published conference papers are welcome **but** there must be at least **40% of new impacting technical/scientific material** in the submitted manuscript. As an author, you are responsible for understanding and adhering to the submission guidelines. You can access them at the IEEE Computer Society web site, www.computer.org. Please thoroughly read these before submitting your manuscript. Please submit your paper to Manuscript Central at https://mc.manuscriptcentral.com/tetc-cs. While submitting through Scholarone, please select the option "Special Section on Emerging Trends and Computing Paradigms for Testing, Reliability and Security in Future VLSI Systems ".

Stefano Di Carlo (https://www.testgroup.polito.it/stefano-di-carlo/) is an associate professor at the department of Control and Computer Engineering at Politecnico di Torino (Italy) since 2014. He holds a Ph.D. (2003) and an M.S. equivalent (1999) in Computer Engineering and Information Technology from the Politecnico di Torino in Italy. Di Carlo's research contributions include Reliability Analysis, FPGA Design, Memory Testing, Reliability analysis of NVM memories with ECC, Design for Testability, Built-In Self-Test, Fault Simulation and Automatic Test Generation.
He has authored 50 transactions/journals papers and >134 peer-reviewed publications in the proceedings of IEEE/ACM sponsored events. He serves on the Editorial Board of top tier journals He has served (and regularly serves) on several Organizing and Program committees of major IEEE and ACM conferences and Symposia. He is the program chair of the IEEE VLSI Test Symposium 2019 and served in the last two years as vice program chair of the IEEE International Symposium on Online Testing and Robust System Design (IOLTS). He coordinated the FP7 CLERECO project. Di Carlo is a Senior Member of the IEEE, and a Golden Core Member of the IEEE Computer Society and receipt of an Outstanding and a Meritorious award for his volunteer activity in the IEEE Computer Society.

Peilin Song (https://researcher.watson.ibm.com/researcher/view.php?person=us-psong) is a Principle Research Staff Member at the IBM Thomas J. Watson Research Center, where he manages the Circuit Diagnostics and Testing Technology department. He joined IBM in 1997 and has since worked in the area of design for testability, fault diagnostics, and recently hardware security and reliability. He has more than 100 publications and holds 59 US patents.

He has served on several Program committees of major IEEE conferences, including IEEE VLSI Test Symposium (VTS) and International Test Conference (ITC). He is the co-Program Chair of 2019 VTS. In 2004, he received the IEEE Electron Device Society (EDS) Paul Rappaport Award. He has been a Golden Core Member of IEEE Computer Society since 2006 and a recipient of the IEEE Computer Society Outstanding Contribution Award in 2006. He received the IEEE 2005, 2006, and 2007 Computer Society Outstanding Contribution and Meritorious Service Awards. In 2015, he received the Paul F. Forman Team Engineering Excellence Award from OSA. He received his Ph.D. in EE from the University of Rhode Island in 1997.

Alessandro Savino (https://www.testgroup.polito.it/alessandro-savino/) is an Assistant Professor at the department of Control and Computer Engineering at Politecnico di Torino (Italy) since 2018.
He holds a Ph.D. (2009) and an M.S. equivalent (2005) in Computer Engineering and Information Technology from the Politecnico di Torino in Italy. His research contributions include Reliability Analysis, Software-Based Self-Test, Approximate computing and Image Analysis.
He has authored several transactions/journals papers and peer-reviewed publications in the proceedings of IEEE/ACM sponsored events. He regularly serves as reviewer of the IEEE Transactions on Reliability, Springer Journal of Electronic Testing: Theory and Applications (JETTA), and several other IEEE journals. He has been Guest Editor for a Special Issue on MDPI Electronics. He has served (and regularly serves) on several Organizing and Program committees of major IEEE and INSTICC conferences and Symposia.